IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A parallel counter comprising:

at least five inputs for receiving a plurality of binary inputs, wherein m represents the number of high binary inputs;

at least three outputs for outputting binary outputs indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of outputs and for generating at least three of the binary outputs as elementary OR or EXOR symmetric functions of the binary inputs, wherein said elementary OR symmetric function is generated by elementary OR symmetric function logic comprising ~~the logic circuit comprises~~ at least one of:

(i) ~~elementary OR symmetric function logic comprising at least one of OR logic for combining binary inputs to generate a binary output which~~ the OR logic combination of the binary inputs and is high if and only if m [[>]] $\geq$1,

(ii) the AND logic combination of ~~for combining~~ sets of the binary inputs and the OR logic combination of ~~for combining~~ the AND logic combinations and ~~combined sets of binary inputs to generate a binary output which~~ is high if and only if m [[>]] $\geq$ k, where k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs, or ~~and~~

(iii) the AND logic combination of the binary inputs and is high if and only if all said binary inputs are high; and said elementary EXOR symmetric function is generated by elementary EXOR symmetric function logic comprising at least one [[of]] of:

(i) the EXOR logic combination of the binary inputs and ~~for combining the binary inputs to generate a binary output which~~ is high if and only if m [[>]] $\geq$ 1,

(ii) the AND logic combination of sets of the binary inputs and the EXOR logic combination of the AND logic combinations and ~~the number of high inputs is an odd number, AND logic for combining sets of binary inputs and EXOR logic for combining the AND logic combined sets of binary inputs to generate a binary output which~~ is high if and only if m [[>]] $\geq$

k and the number of sets of high inputs is an odd number, where k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs, or

(iii) the AND logic combination of the binary inputs and is high if and only if all said binary inputs are high

~~where m is the number of high inputs and k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs~~.

2. (Cancelled)

3. (Cancelled)

4. (Currently Amended) A parallel counter according to claim 1 wherein said logic circuit comprises said elementary [[XOR]] EXOR symmetric function logic ~~includes~~ to generate at least one of:

~~logic to generate~~ the least significant ~~bit~~ of the binary outputs; ~~and~~ or

~~logic to generate~~ the $(i + 1)^{th}$ binary output ~~including logic to AND logic combine~~,

said elementary EXOR symmetric function logic for the $(i + 1)^{th}$ binary output including the AND logic combination of 2^i of the binary inputs in each set ~~and EXOR logic to combine the result of the AND logic combinations,~~ for the generation of the ith binary output where i is an integer from 1 to N-1, N is the number of binary outputs and i represents the significance of a binary output.

5. (Cancelled)

6. (Cancelled)

7. (Cancelled)

8. (Currently Amended) A parallel counter according to claim 1 wherein N is the number of binary outputs, and for the generation of the Nth binary output, said elementary OR symmetric

function logic includes ~~logic to logically AND~~ said AND logic for combining each said set of binary inputs and said OR logic for combining the AND logic combined sets of binary inputs, and wherein the size k of the sets of binary inputs is 2^{N-1} ~~of the binary inputs in each set in the generation of the N^{th} binary output as the elementary OR symmetric function of the binary inputs, where N is the number of binary outputs and the N^{th} binary output is the most significant~~.

9. (Cancelled)

10. (Currently Amended) A parallel counter according to claim 1 wherein ~~said~~ a least significant of said binary outputs is generated as an elementary EXOR symmetric function using said elementary [[XOR]] EXOR symmetric function [[logic]] logic, ~~is adapted to generate a first binary output as an elementary EXOR symmetric function of the binary inputs, and said elementary OR symmetric function logic is adapted to generate an~~ and an N^{th} of said binary outputs is generated as an elementary OR symmetric function ~~of the binary inputs~~ using said elementary OR symmetric function logic, where N is the number of binary outputs and the N^{th} binary output is the most significant.

11. (Currently Amended) A parallel counter according to claim 1 wherein said ~~elementary OR symmetric function logic includes intermediate logic to generate a plurality of~~ logic circuit is arranged to generate two possible binary outputs for a binary output less significant than the N^{th} binary output, as elementary OR symmetric functions of the binary inputs using said elementary OR symmetric function logic for combining a plurality of sets of one or more binary inputs, where N is the number of binary outputs, the sets used for each possible binary output being of two different sizes which are a function of the binary output being generated; and said logic circuit including selector logic to select one of the possible binary outputs based on at least one more significant binary output value.

12. (Currently Amended) A parallel counter according to claim 11 wherein said ~~intermediate logic includes logic adapted to generate~~ logic circuit is arranged to generate said two possible binary outputs for the $(N-1)^{th}$ binary output which is less significant than the N^{th} binary output, as

elementary OR symmetric functions of the binary inputs, the sets used for each possible binary output being of size $2^{N-1} + 2^{N-2}$ and 2^{N-2} respectively, and said selector logic being ~~adapted~~ arranged to select one of the possible binary outputs based on the N^{th} binary output value.

13. (Currently Amended) A parallel counter according to claim 1 wherein said elementary OR or EXOR symmetric function logic ~~and said elementary EXOR symmetric function logic include~~ includes a plurality of subcircuit logic modules each generating intermediate binary outputs as an elementary OR or EXOR symmetric function of some of the binary inputs, and logic for logically combining the intermediate binary outputs to generate said binary outputs.

14-20. (Cancelled)

21. (Currently Amended) A logic circuit for multiplying a first N bit binary number with a second N bit binary number ~~two N bit binary numbers~~, the logic circuit comprising:

array generation logic adapted to generate an array of logical combinations of bits of said first and second N bit binary numbers;

array reduction logic for reducing the depth of the array to two binary numbers; and

addition logic for adding the binary values of the two binary numbers of the reduced array;

wherein said array reduction logic includes at least one parallel counter comprising:

at least five inputs for receiving a plurality of binary inputs, wherein m represents the number of high binary inputs;

at least three outputs for outputting binary outputs indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of outputs and for generating at least three of the binary outputs as elementary OR or EXOR symmetric functions of the inputs, wherein said elementary OR symmetric function is generated by ~~the logic circuit comprises at least one of:~~ elementary OR symmetric function logic comprising at least one [[of]] of:

(i) the OR logic combination of the binary inputs and is high if and only if $m \geq 1$,

(ii) the AND logic combination of sets of the binary inputs and the OR logic combination of the AND logic combinations and is high if and only if m $\geq$k, where k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs, or

(iii) the AND logic combination of the binary inputs and is high if and only if all said binary inputs are high; and said elementary EXOR symmetric function is generated by elementary EXOR symmetric function logic comprising at least one of

(i) the EXOR logic combination of the binary inputs and is high if and only if m $\geq$1,

(ii) the AND logic combination of sets of the binary inputs and the EXOR logic combination of the AND logic combinations and is high if and only if m $\geq$k and the number of sets of high inputs is an odd number, where k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs, or

(iii) the AND logic combination of the binary inputs and is high if and only if all said binary inputs are high

~~OR logic for combining binary inputs to generate a binary output which is high if and only if m >1, AND logic for combining sets of binary inputs and OR logic for combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k, and~~

~~elementary EXOR symmetric function logic comprising at least one of EXOR logic for combining the binary inputs to generate a binary output which is high if and only if m >1 and the number of high inputs is an odd number, AND logic for combining sets of binary inputs and EXOR logic for combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k and the number of sets of high inputs is an odd number, where m is the number of high inputs and k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs~~.

22. (Currently Amended) A logic circuit for multiplying two binary numbers, the logic circuit comprising:

~~an~~ array generation logic adapted to generate an array of logical combinations of bits of binary numbers;

~~an~~ array reduction logic adapted to reduce depth of the array to two binary numbers; and

~~an~~ addition logic adapted to add the binary values of the two binary numbers of the reduced array;

wherein said array reduction logic includes at least one parallel counter comprising:

at least five inputs ~~adapted~~ to receive a plurality of binary inputs, wherein m represents the number of high binary inputs;

at least three outputs adapted to output binary outputs indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of outputs and adapted to generate at least three of the binary outputs as elementary OR or EXOR symmetric functions of the binary inputs,

wherein said ~~logic circuit comprises at least one of: an~~ elementary OR symmetric function is generated by elementary OR symmetric function logic comprising at least one [[of]] of:

(i) the OR logic combination of the binary inputs and is high if and only if $m \geq 1$,

(ii) the AND logic combination of sets of the binary inputs and the OR logic combination of the AND logic combinations and is high if and only if $m \geq k$, where k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs, or

(iii) the AND logic combination of the binary inputs and is high if and only if all said binary inputs are high; and said elementary EXOR symmetric function is generated by elementary EXOR symmetric function logic comprising at least one of

(i) the EXOR logic combination of the binary inputs and is high if and only if $m \geq 1$,

(ii) the AND logic combination of sets of the binary inputs and the EXOR logic combination of the AND logic combinations and is high if and only if $m \geq k$ and the number of sets of high inputs is an odd number, where k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs, or

(iii) the AND logic combination of the binary inputs and is high if and only if all said binary inputs are high;

~~OR logic adapted to combine binary inputs to generate a binary output which is high if and only if m >1, and AND logic adapted to combine sets of binary inputs and OR logic adapted to combine the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k, and~~

~~an elementary EXOR symmetric function logic comprising at least one of EXOR logic adapted to combine the binary inputs to generate a binary output which is high if and only if m >1 and the number of high inputs is an odd number, and AND logic adapted to combine sets of binary inputs and EXOR logic adapted to combine the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k and the number of sets of high inputs is an odd number, where m is the number of high inputs and k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs;~~

wherein said elementary EXOR symmetric function logic is configured to generate ~~includes~~ at least one of:

~~a logic to generate~~ the least significant ~~bit~~ of the binary ~~output~~ outputs; or

~~a logic to generate~~ the $(i+1)^{th}$ binary output, said elementary EXOR symmetric function logic for the (i+1)th binary output including the AND logic combination of ~~logic to AND logic combine~~ 2^i of the binary inputs in each set for the generation of the ith binary output, ~~and EXOR logic to combine the result of the AND logic combinations,~~ where i is an integer from 1 to N-1, N is the number of binary outputs and i represents the significance of a binary output.

23. (Currently Amended) A logic circuit for multiplying two binary numbers, the logic circuit comprising:

~~an~~ array generation logic adapted to generate an array of logical combinations of bits of the binary numbers;

~~an~~ array reduction logic adapted to reduce the depth of the array to two binary numbers; and

~~an~~ addition logic adapted to add the binary values of the two binary numbers of the reduced array;

wherein said array reduction logic includes at least one parallel counter comprising:

at least five inputs adapted to receive a plurality of binary inputs, wherein m represents the number of high binary inputs;

at least three outputs for outputting binary outputs indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of outputs and adapted to generate at least three of the binary outputs as elementary OR or EXOR symmetric functions of the binary inputs,

wherein said elementary OR symmetric function is generated by ~~logic circuit comprises at least one of: an~~ elementary OR symmetric function logic comprising at least one [[of]] of:

(i) the OR logic combination of the binary inputs and is high if and only if m $\geq$1,

(ii) the AND logic combination of sets of the binary inputs and the OR logic combination of the AND logic combinations and is high if and only if m $\geq$k, where k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs, or

(iii) the AND logic combination of the binary inputs and is high if and only if all said binary inputs are high; and said elementary EXOR symmetric function is generated by elementary EXOR symmetric function logic comprising at least one of

(i) the EXOR logic combination of the binary inputs and is high if and only if m $\geq$1,

(ii) the AND logic combination of sets of the binary inputs and the EXOR logic combination of the AND logic combinations and is high if and only if m $\geq$k and the number of sets of high inputs is an odd number, where k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs, or

(iii) the AND logic combination of the binary inputs and is high if and only if all said binary inputs are high;

~~OR logic adapted to combine binary inputs to generate a binary output which is high if and only if m >1, and an AND logic adapted to combine sets of binary inputs and OR logic adapted to combine the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k, and~~

~~an elementary EXOR symmetric function logic comprising at least one of EXOR logic adapted to combine the binary inputs to generate a binary output which is high if and only if m~~

~~>1 and the number of high inputs is an odd number, and an AND logic adapted to combine sets of binary inputs and an EXOR logic adapted to combine the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k and the number of sets of high inputs is an odd number, where m is the number of high inputs and k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs;~~

wherein N is the number of binary inputs, and for the generation of the Nth binary output, said elementary OR symmetric function logic includes said AND logic for combining each said set of binary inputs and said OR logic for combining the AND logic combined sets of binary inputs, and wherein the size k of the sets of binary inputs is ~~to logically AND~~ 2^{N-1} ~~of the binary inputs in each set in the generation of the N^{th} binary output as the elementary OR symmetric function of the binary inputs, where N is the number of binary outputs and the N^{th} binary output is the most significant~~.

24. (Currently Amended) A logic circuit for multiplying two binary numbers, the logic circuit comprising:

~~an~~ array generation logic for generating an array of logical combinations of bits of the binary numbers;

~~an~~ array reduction logic for reducing the depth of the array to two binary numbers; and

~~an~~ addition logic for adding the binary values of the two binary numbers;

wherein said array reduction logic includes at least one parallel counter comprising:

at least five inputs for receiving a plurality of binary inputs, wherein m represents the number of high inputs;

at least three outputs for outputting binary outputs indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of outputs and for generating at least three of the binary outputs as elementary OR or EXOR symmetric functions of the binary inputs,

wherein said ~~logic circuit comprises at least one of: an~~ elementary OR symmetric function is generated by elementary OR symmetric function logic comprising at least one of:

(i) the OR logic combination of the binary inputs and is high if and only if m $\geq$1,

(ii) the AND logic combination of sets of the binary inputs and the OR logic combination of the AND logic combinations and is high if and only if m ≥k, where k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs, or

(iii) the AND logic combination of the binary inputs and is high if and only if all said binary inputs are high; and said elementary EXOR symmetric function is generated by elementary EXOR symmetric function logic comprising at least one of

(i) the EXOR logic combination of the binary inputs and is high if and only if m ≥1,

(ii) the AND logic combination of sets of the binary inputs and the EXOR logic combination of the AND logic combinations and is high if and only if m ≥k and the number of sets of high inputs is an odd number, where k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs, or

(iii) the AND logic combination of the binary inputs and is high if and only if all said binary inputs are high;

~~OR logic for combining binary inputs to generate a binary output which is high if and only if m >1, and AND logic for combining sets of binary inputs and OR logic for combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k, and~~

~~an elementary EXOR symmetric function logic comprising at least one of EXOR logic for combining the binary inputs to generate a binary output which is high if and only if m >1 and the number of high inputs is an odd number, and AND logic for combining sets of binary inputs and EXOR logic for combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k and the number of sets of high inputs is an odd number, where m is the number of high inputs and k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs;~~

wherein a least significant of said binary outputs is generated as an elementary EXOR symmetric function using said elementary EXOR symmetric function logic, and ~~is arranged to generate a first binary output as an elementary EXOR symmetric function of the binary inputs and said elementary OR symmetric function logic is arranged to generate~~ an N^{th} of said binary outputs is generated as an elementary OR symmetric function using said elementary OR

symmetric function logic, where N is the number of binary outputs and the Nth binary output is the most significant ~~of the binary inputs~~.

25. (Currently Amended) A logic circuit for multiplying two binary numbers, the logic circuit comprising:

array generation logic for generating an array of logical combinations of bits of the binary numbers;

array reduction logic for reducing the depth of the array to two binary numbers; and

addition logic for adding the binary values of the two binary numbers of the reduced array;

wherein said array reduction logic includes at least one parallel counter comprising:

at least five inputs for receiving a plurality of binary inputs, wherein m represents the number of high binary inputs;

at least three outputs for outputting binary outputs indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of outputs and for generating at least three of the binary outputs as elementary OR or EXOR symmetric functions of the binary inputs,

wherein said elementary OR symmetric function is generated by ~~logic circuit comprises at least one of:~~ elementary OR symmetric function logic comprising at least one of:

(i) the OR logic combination of the binary inputs and is high if and only if $m \geq 1$,

(ii) the AND logic combination of sets of the binary inputs and the OR logic combination of the AND logic combinations and is high if and only if $m \geq k$, where k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs, or

(iii) the AND logic combination of the binary inputs and is high if and only if all said binary inputs are high; and said elementary EXOR symmetric function is generated by elementary EXOR symmetric function logic comprising at least one of

(i) the EXOR logic combination of the binary inputs and is high if and only if $m \geq 1$,

(ii) the AND logic combination of sets of the binary inputs and the EXOR logic combination of the AND logic combinations and is high if and only if m $\geq$k and the number of sets of high inputs is an odd number, where k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs, or
(iii) the AND logic combination of the binary inputs and is high if and only if all said binary inputs are high;

~~OR logic for combining binary inputs to generate a binary output which is high if and only if m >1, and AND logic for combining sets of binary inputs and OR logic for combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k, and~~

~~elementary EXOR symmetric function logic comprising at least one of EXOR logic for combining the binary inputs to generate a binary output which is high if and only if m >1 and the number of high inputs is an odd number, and AND logic for combining sets of binary inputs and EXOR logic for combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k and the number of sets of high inputs is an odd number, where m is the number of high inputs and k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs;~~

wherein said elementary OR symmetric function logic includes intermediate logic to generate a plurality of possible binary outputs for a binary output less significant than the N^{th} binary output, as elementary OR symmetric functions of the binary inputs, where N is the number of binary outputs, the sets used for each possible binary output being of different sizes which are a function of the binary output being generated; and selector logic to select one of the possible binary outputs based on at least one more significant binary output value.

26. (Currently Amended) A logic circuit according to claim 25, wherein said intermediate logic includes logic to generate two possible binary outputs for the $(N-1)^{th}$ binary output which is less significant than the N^{th} binary output, as elementary OR symmetric functions of the binary inputs, the sets used for each possible binary output being of size $2^{N-1} + 2^{N-2}$ and 2^{N-2} respectively, and said selector logic is arranged to select one of the possible binary outputs based on the N^{th} binary output value.

27. (Currently Amended) A logic circuit for multiplying two binary numbers, the logic circuit comprising:

~~an~~ array generation logic for generating an array of logical combinations of bits of the binary numbers;

~~an~~ array reduction logic for reducing the depth of the array to two binary numbers; and

~~an~~ addition logic for adding the binary values of the two binary numbers of the reduced array;

wherein said array reduction logic includes at least one parallel counter comprising:

at least five inputs for receiving a plurality of binary inputs, wherein m represents the number of high binary inputs;

at least three outputs for outputting binary outputs indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of binary outputs and for generating at least three of the binary outputs as elementary OR or EXOR symmetric functions of the binary inputs,

wherein said elementary OR symmetric function is generated by ~~logic circuit comprises at least one of:~~ elementary OR symmetric function logic comprising at least one of:

(i) the OR logic combination of the binary inputs and is high if and only if $m \geq 1$,

(ii) the AND logic combination of sets of the binary inputs and the OR logic combination of the AND logic combinations and is high if and only if $m \geq k$, where k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs, or

(iii) the AND logic combination of the binary inputs and is high if and only if all said binary inputs are high; and said elementary EXOR symmetric function is generated by elementary EXOR symmetric function logic comprising at least one of

(i) the EXOR logic combination of the binary inputs and is high if and only if $m \geq 1$,

(ii) the AND logic combination of sets of the binary inputs and the EXOR logic combination of the AND logic combinations and is high if and only if $m \geq k$ and the number of

sets of high inputs is an odd number, where k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs, or

(iii) the AND logic combination of the binary inputs and is high if and only if all said binary inputs are high;

~~OR logic for combining binary inputs to generate a binary output which is high if and only if m >1, and AND logic for combining sets of binary inputs and OR logic for combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k, and~~

~~elementary EXOR symmetric function logic comprising at least one of EXOR logic for combining the binary inputs to generate a binary output which is high if and only if m >1 and the number of high inputs is an odd number, and AND logic for combining sets of binary inputs and EXOR logic for combining the AND logic combined sets of binary inputs to generate a binary output which is high if and only if m >k and the number of sets of high inputs is an odd number, where m is the number of high inputs and k is the size of the sets of binary inputs, each set being unique and the sets covering all possible combinations of binary inputs;~~

wherein said elementary OR symmetric function logic and said elementary EXOR symmetric function logic include a plurality of subcircuit logic modules each generating intermediate binary outputs as an elementary OR or EXOR symmetric function of some of the binary inputs, and logic for logically combining the intermediate binary outputs to generate said binary outputs.

28. (Cancelled)

29. (Cancelled)